

Claims

What is claimed is:

- 1 1. A method, comprising:
2 allocating a link from a plurality of memory locations included in a memory
3 segment of a memory to a port at substantially a first time, wherein each of the
4 plurality of memory locations includes a plurality of bits.
- 1 2. The method of claim 1, further comprising:
2 partitioning an information array into at least two segments including the
3 memory segment.
- 1 3. The method of claim 1, further comprising:
2 operating the memory segment as a first-in, first-out resource with respect to
3 the port.
- 1 4. The method of claim 3, wherein operating the memory segment as a first-in,
2 first-out resource further comprises:
3 writing a first datum to be enqueued to the port to a first memory location
4 included in the memory segment;
5 determining an existence of the link; and
6 writing a second datum to be enqueued to the port to a second memory
7 location included in the memory segment.
- 1 5. The method of claim 3, wherein operating the memory segment as a first-in,
2 first-out resource further comprises:
3 reading a first datum to be enqueued to the port from a first memory location
4 included in the memory segment;

5 reading a second datum to be enqueued to the port from a second memory
6 location included in the memory segment; and
7 de-allocating the link.

1 6. The method of claim 1, further comprising:
2 allocating a second link from a plurality of memory locations included in a
3 second memory segment of the memory to the port at substantially a second time,
4 wherein each of the plurality of memory locations included in the second memory
5 segment includes a plurality of bits.

1 7. The method of claim 1, further comprising:
2 determining a maximum hardware utilization as a number of shareable bits
3 divided by a sum of a total number of information bits and a total number of link
4 bits.

1 8. An article comprising a machine-accessible medium having associated first
2 data, wherein the first data, when accessed, results in a machine performing:
3 allocating a link from a first plurality of memory locations included in a first
4 memory segment of a memory to a port at substantially a first time, wherein each of
5 the first plurality of memory locations includes a plurality of bits.

1 9. The article of claim 8, wherein the first data, when accessed, results in the
2 machine performing:
3 choosing a number of the first plurality of memory locations by determining
4 a maximum hardware utilization as a number of shareable bits divided by a sum of a
5 total number of information bits and a total number of link bits.

1 10. The article of claim 8, wherein the first data, when accessed, results in the
2 machine performing:

3 determining that all of the first plurality of memory locations are occupied
4 by second data; and
5 allocating a second link from a second plurality of memory locations
6 included in a second memory segment of the memory to the port at substantially a
7 second time, wherein each of the second plurality of memory locations includes a
8 plurality of bits.

1 11. The article of claim 10, wherein the first data, when accessed, results in the
2 machine performing:

3 determining that none of the second plurality of memory locations are
4 occupied by second data; and
5 de-allocating the second link.

1 12. The article of claim 11, wherein the first data, when accessed, results in the
2 machine performing:

3 allocating the second link to another port.

1 13. The article of claim 10, wherein the number of the second plurality of
2 memory locations is the same as the number of the first plurality of memory
3 locations.

1 14. The article of claim 8, wherein the memory segment is included in a transmit
2 queue storage.

1 15. An apparatus, comprising:

2 a port; and

3 a module to allocate a link from a plurality of memory locations included in
4 a memory segment to the port at substantially one time, wherein each of the
5 plurality of memory locations includes a plurality of bits.

1 16. The apparatus of claim 15, further comprising:
2 a memory comprising a plurality of memory segments including the memory
3 segment.

1 17. The apparatus of claim 16, wherein a number of memory locations in each
2 one of the plurality of memory segments is equal to a number of the plurality of
3 memory locations.

1 18. The apparatus of claim 15, wherein a number of the plurality of memory
2 locations included in the memory segment is chosen in accordance with a maximum
3 hardware utilization substantially equal to a number of shareable bits divided by a
4 sum of a total number of information bits and a total number of link bits.

1 19. The apparatus of claim 15, wherein a number of the plurality of bits is equal
2 to an information array width, and wherein the information array width is about
3 equal to or less than the value of \log_2 of an information array depth.

1 20. A system, comprising:
2 a first port and a second port;
3 a memory coupled to the first port and to the second port; and
4 a module to allocate a first link from a plurality of memory locations
5 included in a first memory segment included in the memory to the first port at
6 substantially a first time, and to allocate a second link from a plurality of memory
7 locations included in a second memory segment included in the memory to the
8 second port at substantially a second time, wherein each of the plurality of memory
9 locations included in the first memory segment and the second memory segment
10 includes a plurality of bits.

1 21. The system of claim 20, further comprising:

2 an omnidirectional antenna to receive information to be stored in the
3 memory.

1 22. The system of claim 20, wherein the memory is to store the first link and the
2 second link.

1 23. The system of claim 20, further comprising:
2 a communications medium to couple the first port to a data switch.